REMARKS

Favorable reconsideration of this application is requested in view of the following remarks. Claims 1, 6, and 11-14 have been amended.

The amendment of claims 1, 11, 12, and 14 reciting when a device on the local bus generates a read cycle to read data from a read address associated with one of the devices on the system bus and the read address is contained in the address stored in the associative memory, the controller reads out corresponding data from the associative memory so as to transfer it to the local bus, is supported, for example, by page 3, lines 23-27. The amendment of claims 6, 13, and 14 reciting when a device on the system bus generates a read cycle to read data from a read address associated with one of the devices on the local bus and the read address is contained in the address stored in the associative memory, the controller reads out corresponding data from the associative memory so as to transfer it to the system bus, is supported, for example, by page 5, lines 17-23.

Claims 1-14 were rejected as being unpatentable over Futral (US 6,317,799) in view of Bauman (US 6,189,078). Applicants traverse this rejection. Futral does not suggest a data transfer apparatus which provides access to data associated with a device on the system bus (local bus according to claims 6 and 13), contained in the associated memory, in response to a read cycle generated by a device on the local bus (system bus according to claims 6 and 13), where a controller reads out the corresponding data from the associative memory and transfers it to the local bus requester (system bus according to claims 6 and 13), as required by claims 1, 11, 12, and 14. Rather, Futral teaches access to an associated memory in response to a **write** cycle generated by a device on the local bus (see column 5, lines 36-46). Futral teaches a queueing buffer for (writing) commands awaiting processing.

Bauman does not suggest that when a device on the local bus generates a read cycle to read data from a read address associated with one of the devices on the system bus and the read address is contained in the address stored in the associative memory, the controller reads out corresponding data from the associative memory so as to transfer it to the local bus, as required

by claims 1, 11, 12, and 14. Rather, Bauman teaches data communication between devices only connected to the same bus (see column 3, lines 43-52). The request for data is not initiated by a second bus, as required by claims 1, 6, and 11-14.

Favorable reconsideration of claims 1-14 is requested.

In view of the above, favorable reconsideration in the form of a notice of allowance is requested. Any questions regarding this communication can be directed to the undersigned attorney, Curtis B. Hamre, Reg. No. 29,165, at (612)455-3802.

Respectfully Submitted,

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